REMARKS

Claims 1-16, 22, 24-26 were pending, of which Claims 9-16, 22 and 25 were indicated as being allowable. Claims 1-3, 8 and 24 were rejected and Claims 4-7 and 26 were objected to. Reconsideration is requested.

Claim Rejections – 35 U.S.C. §102

Claims 1, and 24 were rejected under 35 U.S.C. §102(b) as being anticipated by Nishihara et al. (5,109,430) ("Nishihara"). Applicants request reconsideration.

Nishihara states "We have developed a method for measuring alignment accuracy of overlying layers on integrated circuit structures." Col. 4, lines 61-63. Nishihara is **not** related to de-skewing a wafer or producing a de-skew recipe with learned patters at a de-skew site. Col. 10, lines 50-62 of Nishihara is related to a correlation process that compares an image of a pattern with a stored model of the pattern, where the "difference between the peak positions of these two correlation surfaces represents the alignment error between the two layers." Col. 10, lines 60-62. Thus, Nishihara is measuring the relative displacement between a first layer on a wafer and a second layer. De-skewing and measuring alignment between layers are two fundamentally different things.

Applicants note the similarity between the rejection based on Nishihara and previous rejections based on Hennessey et al. (5,696,835) ("Hennessey"), which the Examiner ultimately withdrew. Applicants refer the Examiner to the discussion of Hennessey in the Applicants' Responses to Office Action dated March 22, 2006 and August 3, 2006. Applicants further note that the Examiner found Applicants' remarks persuasive in the Office Action dated October 20, 2006, and withdrew the rejection.

As with Hennessey, Nishihara is related to measuring the alignment error between two layers on a wafer. Nishihara does not teach or suggest learning first and second patterns at a "de-skew site" or saving the first and second patterns in a "recipe for de-skewing multiple wafer layers".

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Moreover, Nishihara discloses that "a first irregular pattern A" and "a second irregular pattern B" are placed on overlying layers and that "An image of the composite pattern is then acquired and correlated with a stored model of pattern A, then with a stored model of pattern B." Col. 10, lines 53-60. Nishihara does not explicitly or inherently teach or suggest learning

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a first pattern on a first wafer level and saving the first pattern for "de-skewing multiple wafer levels" as recited in claim 1.

Accordingly, Applicants respectfully submit that claim 1 is patentable over Nishihara. Reconsideration and withdrawal of this rejection is respectfully requested. Claim 24 depends from claim 1 and is therefore likewise patentable for at least the same reasons.

Claim Rejections – 35 U.S.C. §103

Claim 8 was rejected under 35 U.S.C. §103(a) as being unpatentable over Nishihara. Applicants respectfully traverse.

Claim 8 depends from claim 1 and is therefore patentable over Nishihara for at least the same reasons as claim 1.

Claims 2 and 3 were rejected under 35 U.S.C. §103(a) as being unpatentable over Nishihara in view of Garakani et al. (6,240,208) ("Garakani"). Applicants respectfully traverse.

Claims 2 and 3 depend from Claim 1. Garakani fails to make up for the deficiencies of Nishihara. Accordingly, Claims 2 and 3 are allowable for at least the same reasons as Claim 1.

For the above reasons, Applicants respectfully request allowance of all pending claims. Should the Examiner have any questions concerning this response, the Examiner is invited to call the undersigned at (408) 378-7777.

CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that this correspondence is being facsimile transmitted to the U.S. Patent and Trademark Office to the fax number 571-273-8300 on February 21, 2008.

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